The Silicon tracking systems in the Linear Collider Detector Concepts

This presentation is mostly based on the work and ideas that are being developed within the SiLC (Silicon tracking for Future Colliders) R&D International Collaboration and with the detector concepts for ILC, CLIC also in strong synergy with the LHC experiments construction and their forthcoming tracking upgrades.
SiLC (Silicon tracking for Linear Collider)

**Goal:** To develop the next generation of large area Silicon trackers

**Strong synergy** with the construction of LHC Si trackers & their upgrades

Opening since last year to the CLIC case.

Currently 3 LOIs and Detector concepts and 3 tracking concepts
Two tracking strategies

All Silicon tracking

Combined Silicon & gaseous tracking

Two integration solutions: Differences but still many common issues
An All Silicon tracking case

~100 m$^2$ Si Strips: Barrel single sided ($r$-ϕ); end caps double sided

Modular low mass sensors tile CF cylinders

Double-metal readout traces

Kapton cable

1024-channel KPiXs

~10 cm x 10 cm; 320 µm thick; 25 µm sense pitch; 50 µm readout (prototype fabricated);

S/N > 20; <5 µm hit resolution

Bump bonded readout with 2 KPiX chip; no hybrid

KPiX measures amplitude and bunch # in ILC train, up to 4 measurements per train

Pulsed Power: 20 µW/channel avg; ~600 W for 30 M channels; gas cooling

(From SiD LOI talk-TILC09)
The inner tracking part of SiD

In their latest designs, all ILC detector concepts are introducing a few more forward disks in order to ensure the tracking coverage down to very low angle w.r.t beam axis (see also 4th).

Around the beam pipe two 4-plane end disk assemblies and three additional disks per end for extended coverage.

All elements are supported indirectly from the beam tube via double-walled, Carbone fibre laminate half cylinder.

Sensor thickness of 75 μm assumed, with 20 x 20 μm² pixel size

(Courtesy M. Demarteau)
Let’s think a bit different...

An all Si tracking a bit different from SiD
Within SiLC some teams (LPNHE, OSU) are revisiting the All-Silicon tracking; the goal is to come up with a new design. The tools are developed and simulations studies are starting.

or REALLY different from SiD (all pixels)

An all Silicon pixel tracking area => gives $30 \times 10^{9}$ pixel channels

*What looks a bit crazy today will be just standard (after) tomorrow... (proposed by SiLC (BILB07) and now C. Damerell)*
Presently under study 7 layers as follows: DSSD, DSSD, SSD, SSD, DSSD, SSD, SSD. The double sided layers are currently XY. There are 4 layers in the End Cap with 2 possible designs; XUV or XY. The overall concept design will be studied/optimized with detailed simulation studies and a full Silicon tracking reconstruction.
Silicon Pixel Tracker

- Barrel + Forward trackers area = 70.3 m²
- With 50 × 50 μm² pixels: **28.1 Gpix system**
- If each chip is 8 cm × 8 cm (2.6 Mpix):
  => **11,000 sensors is total**

- SiC foam support ladders, linked mechanically to one another along their length
- 5 closed cylinders (incl end caps, not shown) will have excellent mechanical stability
- ~0.6% $X_0$ per layer, 3.0% $X_0$ total, over full polar angle range, plus <1% $X_0$ from VXD system (goal)
- 30 Gpixels, in line with trends in astronomical wide-field focal plane systems by 2020

*Courtesy of Ch. Damerell, Warsaw 2008*
The ILD case: combined Silicon + TPC tracking

In order to exploit the combined benefits of these 2 tracking techniques
Integration of a Silicon system into the ILD concept: remarks

The construction and the integration of a Silicon tracking system, part of an hybrid tracking ensemble (CDF, ATLAS) is much more challenging than an all-Silicon fully integrated system (CMS, SiD and future s-ATLAS). Among the main challenging issues:

Ọ THE SPACE ALLOCATED:
An all-Silicon system has all the tracking space for it alone (1.2m radius or so)
Hybrid: only 2cm for the SET, 4cm for the ETD, 20-25cm for SIT+FTD

Ọ THE FIXATION and SUPPORT STRUCTURE:
All Si can build the support structure as desired as well as its own fixing system.
Hybrid: the Si device fully depends on the restricted space and the surroundings.

Ọ THE ROLE:
All Silicon system must primarily fulfill the role of a highly performing tracker i.e. in momentum and spatial resolution measurements.
Hybrid case: the Si component must provide additional functions: alignment, time stamping, handling of distortions of the gaseous detector etc....

Ọ ALIGNMENT: “global” in the all Si case, “mixed-mode” in the hybrid case.
Ọ COOLING: here also much more constraining in the hybrid case (much more dependant on the neighbors)
The Silicon Envelope (current scheme)

**The Envelope: WHY?**
- Improved tracking performances
- Tracking Hermiticity
- Monitoring, Alignment & Distortions
- Robustness, Liability, Redundancy

Detailed design GEANT4 simulation both in MOKKA & ILCROOT (here) & mechanical design (CATIA) in progress

ILD

Si tracking for LC
ILD inner Si tracking system

7 FTD disks, presently: 3 first = pixels, the other 4 are made of 16 petals with DSS strip sensors (similar to FWD ATLAS).

 Possibly later: all pixels (?)
SIT: Silicon Internal Tracker

SIT is made of 2 false double sided X,Y layers (built in the same way than SET) The SIT design as described by A. Charpy with ILCROOT simulation includes:

SIT1: 99 modules made each of a single sensor and 33 modules of 3 sensors each.
SIT2: 270 modules made each of a single sensor and 90 modules of 3 sensors each.
The VTX is fixed to the beam pipe and includes its own envelope.
The SIT and FTD are fixed to the support structure which itself will be fixed to the TPC: middle plan and on the two edges.
There is for ALL the Silicon components only one cable path, i.e. the one along the beam pipe as sketched here below.

SUPPORT STRUCTURE OF SIT+FTD

Courtesy of M. Jore
Towards engineering design of the Forward

Three first disks, nearer to IP made of pixels, 4 last disks made of DSSD strip detectors
ALIGNMENT in innermost region (IMB-CNM & ICFA)

Concept of IR alignment system: use IR beams as infinite momentum tracks. (AMS, CMS)

Selected sensors are traversed by IR beams. These beams are then measured as particle tracks and a first order alignment scenario is obtained. The rest of sensors are aligned using particle tracks. The transference of coordinates from optical aligned to track aligned modules is done via sensor overlap.

Collimator heads on 1st wheel produce IR-tracks that sequentially cross several Si sensors.

Precision: 2μm.

This alignment system will be used for both SIT and FTD.

Slide from Marcos Fernandez Garcia (IFCA)
Nobody is perfect ....

Drift chamber efficiency vs. theta

Momentum resolution vs. theta

Need also further forward coverage

Courtesy F. Grancagnolo (CLUCOU in 4th)

Si tracking for LC
The mechanical structure of the SET is studied in details by the Torino team a real progress was made these last few months.

After a certain number of preliminary designs and studies, P. Mereu and D. Gamba have come to the following basic design:

The mechanical structure of the SET is made by 2 halves composed of 24 panels 2,4x0,48m. Each panel is independently fixed at both short sides to the outer surface of the TPC structure, thus avoiding an additional outer frame and therefore keeping the material budget at its minimum.

Static deflection with a payload of 1kg/m² is given in the following slide.

Silicon detectors are fixed on the surface of each panel; details of this fixation are being studied.
Each panel is independently fixed at both short sides to the outer surface of the TPC structure.

2 halves composed of 24 panels 2.4x0.48m. 
Torino will build such a panel as demonstrator and to study all related issues.
5/7/2009

Si tracking for LC

Scale in meters

3.8 m
SET: Study of design implementation with detailed simulation

Presently SET is made of false double sided Silicon layers equipped with basic modules made of 5 sensors on both X,Y directions

Challenging issues: alignment (the positioning on the TPC wall must be precise at 100µm) well monitored wrt SIT could/should be refined with a few tens of µm (under study).

Power dissipation from calorimeters? Vibrations? Etc... Issues to be studied.

A. Charpy (LPNHE)

ILCROOT simulation
ETD integration in the end cap and Very Forward calorimeter region

ETD studied at LPNHE: A. Charpy, P. Ghislain, D. Imbault, ASN and with M. Jore, R. Poeschl (LAL), P. Anduze (LLR) & D. Grondin (LPSC)

ILD EndCap design
Design courtesy of M. Jore
The endcap issue: TPC vs CLUCOU

After the TPC end cap, one XUV (instead of projective geometry: much simpler design, similar to barrel SET) triplet is included. The XUV serves as “entry point” for ECAL; as an alternative 2 XY plans (-> track segment) is also studied.

ILD: TPC End Plate=> **15% X0**

CLUCOU different case: **3% X0** in end cap; study just starting
One XUV quadrant end cap: present design

Made of modules with 2 (yellow) or 3 (green) sensors. (current design, rapidly evolving)
12 quadrants per XUV triplets. Thus 24 in total. Fixed via a C fibre membrane to the e.m. calorimeter; Positioning screw with precision of the order of 100 μm, light but very precise.
A mechanical prototyped quadrant will be built and tested with mechanical proto of e.m.
End Cap: the XUV design studies

Single sensor modules; 2-sensors; 3 sensors
Detailed simulation of a single plan of the XUV triplet: 4 quadrants

The three XUV plans superimposed And showing the 30° angle symmetry
Two XY plans alternative

The zone around the central hole will be covered by pixels in the XUV case (central blue zone)

Superimposing XY vs XUV

2 XY plans (X and Y ensure no dead region between them)
### The Silicon Envelope in numbers (current scheme)

<table>
<thead>
<tr>
<th>Component</th>
<th>Layer #</th>
<th># modules</th>
<th># sensors/module</th>
<th># channels</th>
<th>Total surface m²</th>
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<tbody>
<tr>
<td>SIT1</td>
<td>1st layer</td>
<td>33</td>
<td>3</td>
<td>66.000</td>
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<tr>
<td></td>
<td>2nd layer</td>
<td>99</td>
<td>1</td>
<td>198.000</td>
<td>0.9</td>
</tr>
<tr>
<td>SIT2</td>
<td>1st layer</td>
<td>90</td>
<td>3</td>
<td>180.000</td>
<td>2.7</td>
</tr>
<tr>
<td></td>
<td>2nd layer</td>
<td>270</td>
<td>1</td>
<td>540.000</td>
<td>2.7</td>
</tr>
<tr>
<td>SET</td>
<td>1st layer</td>
<td>1260</td>
<td>5</td>
<td>2.520.000</td>
<td>55.2</td>
</tr>
<tr>
<td></td>
<td>2nd layer</td>
<td>1260</td>
<td>5</td>
<td>2.520.000</td>
<td>55.2</td>
</tr>
<tr>
<td>ETD_F</td>
<td>X or U or V</td>
<td>82/quad =328/layer =984/ETD</td>
<td>2 or 3 or possibly 4</td>
<td>2.000.000</td>
<td>30</td>
</tr>
<tr>
<td>ETD_B</td>
<td>idem</td>
<td>idem</td>
<td>idem</td>
<td>idem</td>
<td>30</td>
</tr>
</tbody>
</table>

Total number of channels:
$$10^6 \text{ (SIT)} + 5 \times 10^6 \text{ (SET)} + 4 \times 10^6 \text{ (2 ETD)} = 10 \times 10^6 \text{ channels}$$

Total area:
$$7 \text{ (SIT)} + 110 \text{ (SET)} + 2 \times 30 \text{(ETDs)} = 180 \text{ m}^2$$

Total number of modules:
$$500 \text{ (SIT)} + 2500 \text{ (SET)} + 2000 \text{ (ETDs)} = 5000 \text{ modules with unique size sensors}$$

=> Achieved: a unified and simple design for all components (except FTD)
Common issues and challenges

- The basic module (see next slides)
- The sensors (see next slides)
- The forward Si tracking (converging scheme) ✅
- The FEE and direct connection to the sensor (see next slides)
- Power cycling (next slides)
- Effect of high B-field (vibrations): NOT YET (will be tested with new chips)
- The support structures ✅
- The modularity: ✅
  - towards a unique sensor type in the present ILD design for all components but FTD and repetitive elements of construction (super-modules): ✅
  - or a unique module size (SiD) at least in the central barrel (the End Caps:??): ✅
- The cooling (studies ongoing since a few years on Si prototypes –SILC- need combined tests with other sub-detectors mechanical prototypes (foreseen)
- The alignment techniques ✅
- The stability, robustness, reliability (under study)
- Calibrations, monitoring, push pull issues (under study or development)

Even if alternatives are looked for by the different detector concepts, the issues and often the solutions to them are rather similar. A lot of work underway within SiLC.

A few examples have been already shown and a few more here after.
Present status (left) vs next step:

DSM-FE readout into one single unit:
- 8-256ch chips
- Total size: 8x0.5 cm²
- Thinned: 50µm
- Directly connected onto the sensor
- No more pitch adapter,
- No more hybrid board
- Change in the cabling technology

KEY-PIECE of Si tracking:
THE BASIC MODULE

FE readout ASIC (total 2000ch)

Cabling daisy chain with other modules
SiLC (ILD) develops very light modules, with edgeless sensors (no overlay => challenging alignment btw modules) & variable strip length (exploit ILC cycle) thus reduction of electronic channels.

SiD: unique barrel tile: a bit more conservative

SPACE FRAME: the solution?

Detailed architecture of the support structure in progress at ILD.
Super-module to be built by Torino (SET) & Paris(ETD) for studying the pending issues
R&D on sensors roadmap

- **Strip sensors: in progress**
  - “Standard strips” but: larger wafers 6” → 8”, thinner: 300 → 200μm, pitch: 50 μm
  - **Edgeless:**
    - Planar 6”, 50 μm pitch,
    - ≤ 200 μm thick and go to 3D (next slide)

- **Strip sensors for alignment: in progress**
  - Standard specially treated
  - Novel technology

- **Smaller sensors granularity** (also wrt CLIC)
  - follow SLHC developments ex: strixels
  - **Pixels:** 3D technology based (Low Material Budget & High Gain Pixels by OSU) & joining the worldwide effort

- **Inherited expertise** on detailed testing: **test structures**
- **Newly developed** refined tests at the **test beams**

Si tracking for LC
NEW SENSORS R&D: R&D on 3D planar & 3D strips (by 2011-12?)

Fabrication

- 2 batches under fabrication at FBK

1) Recycle of 3D-DTC-2: n-on-p, 200-μm thick substrate, non-passing-through columns (180 μm)
   Currently at 2nd DRIE etching, to be completed by 02/09.

2) 3D-DTC-3: n-on-p, 250-μm thick substrate, full 3D detectors (passing-through) columns.
   New double-sided process defined, no need for support wafer, also suitable for dual read-out pixel/strip.
   Just started, to be completed by 04/09

Column overlap not optimized: about 60μm

Courtesy G. F. Dalla Betta
3D-DTC-2 batch

- P-type substrate
- ATLAS pixels
- CMS pixels
- Test structures

Column overlap still not optimized: about 100um
IMB-CNM (Barcelona) is producing the first sensor prototypes with multi-geometry and optimum thickness. Tentatively scheduled for test beam in August 2009 (?)

Alignment sensor 1.5\(\times\)1.28 cm\(^2\) (256 strips\(\leftrightarrow\)2 Alibava)
(Likely to become 1.5\(\times\)1.5 cm\(^2\) with guard rings...)

Al hole in the back \(\sim\)1 cm
Strip width is the same along the full strip
Slightly larger area to mount on PCB

Optical test structure (TS)

No Al in the back
1 per layer of material
Ellipsometry?

Electrical TS
See poster by M. Dragicevic at INSTR08, Novosibirsk

All SiLC TS are valid here

Pitch=50 \(\mu\)m
Metal width=3, 5, 10, 15 \(\mu\)m

AC sensors
– Al strips
– Al strips&Al backside

Granted by GICSERV08

(Pictorial view)

New Sensors R&D (cont’d)
NEW 3D PIXELS: LOW MATERIAL BUDGET & HIGH INTRINSIC GAIN (OSU)

Microcells operating @ breakdown mode
Gain up to 10**6
Thickness down to a about 10 microns
Size of pixels 10x10 up to 100x100 μm
Electronics can be implemented onto the detector
Test bench to measure sensor detailed performances

New series of tests in 2009 at CERN with novel sensors from IMB-CNMI and from Poland with wire bonded chips. Expertise & experienced teams: asset

HEPHY VIENNA
Th. Bergauer, S. Haensel, M. Krammer et al. (HEPHY)

SPS-CERN

HEPHY VIENNA

(CU Prague)

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<td>2721</td>
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Resolution (µm)

0 intern strips  1 intern strip  2 intern strips
Si Tracking FEE challenges at ILC

The ILC machine cycle imposes the running condition of the detectors/electronics:

- Long shaping time (slow machine)
- Power cycling (possible)
- Digitization and pre-processing: Taking advantage of time between inter-bunch trains

Two tracking concepts:
- A Silicon Envelope around the central gaseous device (ILD case)
- An all Silicon tracker (SID case)

Up to $30 \times 10^6$ Silicon strips (readout channels)
- strip length $< 30$ cm
- Thickness $< 300 \, \mu$m
- readout pitch $50 \, \mu$m

AC coupled (DC coupled if necessary)

$\rightarrow$ Tens of Millions of channels
Integration of k-scale channels readout chip

5/7/2009
Front-End chip numbers

- **Goal:** Integrate 512-1024 channels in 90nm CMOS:
  (but foreseen elementary blocks of 256 channels: multiplexing factor 256:1)

- Amplifiers: 30 mV/MIP over 30 MIP range
- Shapers: 500ns–2μs
- Sparsifier: Threshold the sum of 3-5 adjacent channels
- Samplers: 8 samples at variable sampling clock period (up to 80ns)
  Event buffer 8 depth
- Noise baseline: at least as good as measured with 180nm CMOS:
  375 + 10.5 e-/pF @ 3 μs shaping, 210μW power
- ADC: 12 bit-ADC
- Buffering, digital pre-processing
- Calibration
- Power switching can save a factor of about 70

ILC timing: 1 ms: ~ 2820 trains @ 337ns / BC  200ms in between
R&D on Electronics

Developing a mix-mode FE readout with pulse-height reconstruction, zero suppression, full digital control (highly fault tolerant, flexible/robust) power cycling, in DSM CMOS tech.

Roadmap on Electronics

- Go to 256 channels
- Thinning
- Go to 90 nm CMOS techno
- Direct connection of the FE chip onto the strip sensor (wire bonding->bump bonding -> 3D interconnect)
- Adapting FE to CLIC cycle (complete revisit of FE)
- Bunch tagging at CLIC
- Develop the TOT
- Develop the Data processing and data handling (DAQ)

SiTR_130-88 just developed. New version with 128 channels to equip test beam prototypes (2010), in progress.
Test of the analogue part

Measured power dissipation per ch (all the analog chain up & A/D included): ~1.35mW/channel

Measured gain ~ 43mV/MIP @ 2.6% of nonlinearity up to 24MIP

Output signal of the preamplifier and the shaper as seen at the oscilloscope

N.B. very preliminary lab test measurement but it already shows a good agreement with simulation

Linearity of the preamplifier and the shaper
Machine cycle: CLIC vs ILC

ILC
- 200 ms
- bunch crossing at 337 ns
- 0.950 ms

CLIC
- 20 ms
- bunch crossing at 0.67 ns

50 Hz Repetition Rate

~ 100 ps

500.2 ps, 1999 MHz

5/7/2009
Main parameters for tracking at CLIC

- Need time stamping with high precision (bunch crossing 0.67ns)
- Need double hit recognition for the tracking
- Fast shaping time and requirements on other conditions imply that shorter strips or even pixelization are required.
- New developments on TPC => TPC is back again in the game thus 2 scenarios:
  - All Silicon tracker
  - Silicon +TPC (DC??) tracker

These 2/3? alternatives are studied for CLIC. **But CLIC will be quite different wrt the ILC case and so the detectors (see list above).**

*Since CLIC08 Workshop at CERN, SiLC officially stated that it will study the Silicon tracking for CLIC case (invited talk at CLIC08-CERN).*
FEE challenges at CLIC

- Fast VFE (type LHC or even faster), i.e. fast shaping
- Power dissipation increase
- Higher number of channels to read
- Time stamping with dedicated FE to 100ps or less.
- Power cycling: looks possible but tp be done ??
- Pulse height reconstruction: ideas derived from previous experience in RD16 (LPNHE) but ???

A very exciting and new field is opening in the FE field. SiLC is starting to address these issues...
Both ILC and now CLIC claim there will be two detectors but only one interaction region => the push pull nightmare or all detectors Apart from the more than challenging mechanical aspects, it will dramatically increase the stress on calibration, monitoring of all kinds and especially on alignment for the tracking devices that are most demanding in terms of accuracy of alignment A totally new field for all of us !

One of the important R&D topics especially for the tracking systems with many different facets. And also an advocacy for detection systems designs and functioning as simple as possible.
Combined tests with EUDET Telescope - SPS CERN

EUDET Telescope

Si prototype read out by new FE chip

LPNHE
CU Prague
IFCA
TORINO

Signal to noise ratio: Chip 1

Entries: 17,452
Mean: 2.574
RMS: 4.882
$\chi^2$/ndf: 132.5/105
Width: 0.2936 ± 0.0618
MPV: 23.4 ± 9.1
Const.: 89.48 ± 3.73
Sigma: 1.349 ± 0.279

Resolution (µm)

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Silicon tracking prototype with complete test infrastructure (standalone)

- 5 Si-HPK strips modules (LPNHE+CERN bonding Lab)
- Alignment sensors (IFCA-HPK)
- Faraday cage (DESY+LPNHE)
- Automation 3D table (Torino)
- FPGA-board: 2VA1 modules (1024 ch) + 3 SiTR_130-88 modules (1056 ch) (LPNHE)
- Trigger counters (CU Prague)

PS-CERN, Nov 1-7 2008
Combined tests with TPC prototype at DESY (HEPHY, IEKP, LPNHE new chips)

Mechanical support

challenging task
• little space (2 x 35mm) between TPC and magnet
• silicon detectors must be moveable in both z and phi because the sensors have to stay in the beam during magnet and TPC movements

wire bonds to connect the different parts with each other

silicon sensors
Kapton Foil
hybrids housing the front end electronics
Concluding remarks

- The LOI gave a serious boost in developing realistic scenarios for integrating the Si tracking in the various detector concepts.
- Two Si tracking scenarios: with or without gaseous detector; The all-Si case is much simpler for integrating than the hybrid or combined case.
- But there are many common issues with often similar solutions in both schemes.
- This reinforces the interest of having an horizontal R&D that addresses these issues on common basis and gather the efforts of many teams to work on the best possible solutions. This is what SiLC is doing.
- Moreover the test beams and prototypes developments are instrumental as well as the combined tests with other sub-detectors. There also an horizontal R&D helps in merging the efforts.
- SiLC has accomplished a long way since it started in 2002 and was first submitted to PRC-DESY in 2003. It is considered as one of the preeminent R&D for LC and this has been recognized at the TILC09 workshop. The fact that the all Silicon envelope is part of the reference design of ILC is another proven success.
- The dynamics created with the LOIs should not be lost!! And synergy with LHC and upgrades should be reinforced even more when considering CLIC. This R&D topic is among the crucial one of this forthcoming decade and will witness a lot of progress because of its close connection and large impact on the high tech domain.
By Rolf Heuer some years ago...